

SPECIAL SEMINAR

REVOLUTIONARY SILICON ‘ANCILLARY’ TECHNOLOGIES AND ARCHITECTURES FOR THE NEXT ERA OF GIGASCALE SYSTEMS

Muhammad S. Bakir
Microelectronics Research Center
Georgia Institute of Technology

Abstract

The information revolution has been the most important economic event of the past century and its most powerful driver has been the silicon integrated circuit (IC). Over the past fifty years, the migration from BJT to CMOS technology combined with transistor scaling has produced exponential benefits in microchip productivity and performance. However, as gigascale silicon technology progresses beyond the 45 nm node, the performance of a system-on-a-chip (SoC) has failed by progressively greater margins to reach the “intrinsic limits” of each particular generation of technology. The root cause of this failure is the fact that the capabilities of monolithic silicon technology per se have vastly surpassed those of the ancillary or supporting technologies that are essential to the full exploitation of a high performance SoC, especially in areas of cooling, off-chip signaling, and power delivery. Revolutionary silicon ancillary technologies are urgently needed to address these limits on 2D and 3D gigascale systems. In this presentation, I will discuss novel electrical, optical, and ‘thermal’ interconnect and system integration technologies to address the above grand challenges. The electrical interconnects provide power delivery and signaling, the optical interconnects support massive off-chip (3D stack) bandwidth, and the ‘thermal’ interconnects (based on micro-liquid cooling) provide heat rejection from a 3D stack of high-performance chips (interlevel cooling). The overarching strategy of this novel research is to extend and utilize low-cost wafer-level batch processing, the key to the success of Si technology, to the ancillary technologies that have now become the “*millstone around the neck of Si technology itself.*” Compact physical modeling, trade-off analysis, and the impact of these technologies on microchip and system performance are also presented.

Speaker’s Biographical Sketch

Muhammad S. Bakir received the BEE degree from Auburn University, Auburn, AL, in 1999 and the MS and PhD degrees from Georgia Tech in 2000 and 2003, respectively. He is currently a researcher at the Microelectronics Research Center at Georgia Tech. His areas of interest include integrated electrical, optical, and fluidic interconnections for 3D gigascale integration, power delivery, advanced cooling, chemical and biological sensors, system integration and architecture, and nanofabrication technology. He has published more than 60 refereed and invited publications that appear in conference proceedings and journals and holds nine US patents. He also presented an invited forum presentation at the 2007 *IEEE Int. Solid State Circuits Conf.* (ISSCC). He has edited a book entitled *Integrated Interconnect Technologies for 3D Nanoelectronic Systems* (Artech House, Nov. 2008; co-editor: James Meindl) and is the recipient of the *Best Invited Paper Award* from the 2007 *IEEE Custom Integrated Circuits Conference* (CICC), the *Best Paper Award* from the 2002 *Electronic Components and Technology Conference* (ECTC), the *Outstanding Paper Award* from the 2007 *Electronic Components and Technology Conference* (ECTC), and the co-recipient of the *Best Student Paper Awards* from the 2005 and 2006 *IEEE International Interconnect Technology Conference* (IITC). He is a member of the International Technology Roadmap for Semiconductors (ITRS) technical working group for Assembly and Packaging (AP).

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