

Alex K. Jones

CONTACT INFORMATION

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PROFESSIONAL INTERESTS

Compilation techniques and novel architectures for ASICs, FPGAs, SoCs such as coarse-grain reconfigurable fabrics, interconnections for multi-processor SoCs, RFID, and nanotechnology inspired structures particularly targeting low-power and high-performance. Other interests include increasing usability of traditional CAD techniques and tools, parallel-computing, and software engineering.

EDUCATION

Ph.D. September 2002, Northwestern University, Department of Electrical and Computer Engineering, Evanston, Illinois. Dissertation title: "PACT HDL: A C Compiler Targeting ASICs and FPGAs with Power and Performance Optimizations." Advisor: Prithviraj Banerjee.

M.Sc. September 2000, Northwestern University, Department of Electrical and Computer Engineering, Evanston, Illinois. Specialization: Computer-aided design and Parallel FPGA design.

B.Sc. May 1998, The College of William and Mary, *cum laude*, Major: Physics, Secondary Major: Music Performance. Thesis: Acoustic Music Synthesis, *high honors*.

PROFESSIONAL POSITIONS HELD

Assistant Professor, September 2003 - *current*: Department of Electrical and Computer Engineering, University of Pittsburgh, Pittsburgh, Pennsylvania.

Assistant Professor, September 2005 - April 2006: Department of Computer Science, University of Pittsburgh, Pittsburgh, Pennsylvania - *Secondary Appointment*.

Visiting Researcher, 8/2003-9/2003: Department of Electrical Engineering, University of Pittsburgh, Pittsburgh, Pennsylvania.

Instructor, 9/2002-6/2003: Electrical and Computer Engineering, Northwestern University, Evanston, Illinois. Responsible for teaching core undergraduate and graduate courses in computer engineering, specifically, digital design, parallel computing, computer architecture, and computer-aided design.

Research Associate, 9/2002-7/2003: Center for Parallel and Distributed Computing (CPDC), Northwestern University, Evanston, Illinois. Post doctoral research responsibilities including research management and advising of M.Sc. and Ph.D. students, writing and reviewing papers, grant writing and review, and conducting original research.

HONORS AND AWARDS

Promoted to Senior member of the IEEE, July, 2008.

Pitt Innovator Award, 2007.

Featured Paper, Journal of Low Power Electronics, No. 1, Vol. 3, December 2005.

Walter P. Murphy Doctoral Fellowship, Northwestern University. Awarded twice in 1998 and again in 2000.

Best Paper Award Nominee, IASTED PDCS Conference, 2001, 2003.

Intel Fellowship Nominee.

Graduated *cum laude*, The College of William and Mary, 1998.

Received *high honors* for senior research in Acoustic Music Synthesis as part of my B.Sc. in Physics from the College of William and Mary.

PUBLICATIONS

REFEREED JOURNAL PUBLICATIONS

1. S. Shao, Y. Zhang, A. K. Jones, and R. Melhem, *Symbolic Expression Analysis for Compiled Communication*, Parallel Processing Letters, – *in press*.
2. R. Hoare, Z. Ding, and A. K. Jones, *A Near-optimal Two-stage Hardware Scheduler for Large Cardinality Crossbar Switches*, Journal of Parallel and Distributed Computing (JPDC) - *in press*.
3. A. K. Jones, G. Mehta, J. Stander, M. Baz, and B. Hunsaker, *Interconnect Customization for a Hardware Fabric*, ACM Transactions on Design Automation for Electronic Systems (TODAES) - *in press*.
4. S. Dontharaju, S. Tung, J. T. Cain, L. Mats, M. H. Mickle, and A. K. Jones, *A Design Automation and Power Estimation Flow for RFID Systems*, ACM Transactions on Design Automation for Electronic Systems (TODAES) - *in press*.
5. S. Shao, A. K. Jones, and R. Melhem, *Compiler Techniques for Efficient Communications in Circuit Switched Networks for Multiprocessor Systems*, IEEE Transactions for Parallel and Distributed Systems - *in press*.
6. A. K. Jones, R. A. Walker, *Introduction to the Special Issue on Demonstrable Software Systems and Hardware Platforms II*, ACM Transactions on Design Automation for Electronics Systems (TODAES), Vol. 13, No. 3, Article 38, July, 2008, DOI 10.1145/1367045.1367047.
7. A. K. Jones, S. Dontharaju, S. Tung, L. Mats, P. Hawrylak, R. R. Hoare, J. T. Cain, and M. H. Mickle, *Radio Frequency Identification Prototyping*, ACM Transactions on Design Automation for Electronic Systems (TODAES), Vol. 13, No. 2, April, 2008, pp. 1-21, Article 29, DOI 10.1145/1344418.1344425.
8. M. H. Mickle, J. T. Cain, A. K. Jones, *Intellectual Property and Ubiquitous RFID*, Recent Patents on Electrical Engineering, Vol. 1, No. 1, January 2008, pp. 59-67.
9. A. K. Jones, R. Hoare, S. Dontharaju, S. Tung, R. Sprang, J. Fazekas, J. T. Cain, M. H. Mickle, *An Automated, FPGA-based Reconfigurable, Low-Power RFID Tag*, Journal of Microprocessors and Microsystems, Vol. 31, No. 2, March 2007, pp. 116-134.

10. S. Dontharaju, S. Tung, A. K. Jones, L. Mats, J. Panuski, J. T. Cain, and M. H. Mickle, *The Unwinding of a Protocol*, IEEE Applications and Practice - April, 2007, Vol. 1, No. 1, pp. 4-9.
11. A. K. Jones, R. Hoare, D. Kusic, J. Fazekas, G. Mehta, and J. Foster, *A VLIW Processor with Hardware Functions: Increasing Performance While Reducing Power*, IEEE Transactions on Circuits and Systems II, Vol. 53, No. 11, November 2006, pp. 1250-1254.
12. A. K. Jones, S. Dontharaju, S. Tung, P. Hawrylak, L. Mats, R. Hoare, J. T. Cain, M. H. Mickle, *Passive Active Radio Frequency Identification Tags (PART)*, International Journal of Radio Frequency Identification Technology and Applications (IJRFITA) - Vol. 1, No. 1, 2006, pp. 52-73.
13. J. M. Lucas, R. Hoare, I. S. Kourtev, A. K. Jones, *Technology Mapping for Field Programmable Gate Arrays using Content-Addressable Memory (CAM)*, Journal of Microprocessors and Microsystems - Vol. 30, No. 7, November, 2006, pp. 445-456.
14. A. K. Jones, R. Hoare, D. Kusic, G. Mehta, J. Fazekas, and J. Foster, *Reducing Power while Increasing Performance with SuperCISC*, ACM Transactions on Embedded Computing Systems (TECS) - Vol. 5, No.3, August 2006, pp. 658-686.
15. J. Schuster, K. Gupta, R. Hoare, and A. K. Jones, *Speech Silicon: An FPGA Architecture for Real-time, Hidden Markov Model Based Speech Recognition*, EURASIP Journal on Embedded Systems (JES), Vol. 2006, Article ID 48085, 2006, Pages 1-19.
16. G. Mehta, R. R. Hoare, J. Stander, J. Lucas, B. Hunsaker, and A. K. Jones, *A Low-Energy Reconfigurable Fabric for the SuperCISC Architecture*, Journal of Low Power Electronics (JOLPE) - Vol. 2, No. 2, August 2006, pp. 148-164.
17. P. J. Hawrylak, L. Mats, J. T. Cain, A. K. Jones, S. Tung, M. H. Mickle, *Ultra Low-power Computing Systems for Wireless Devices*, International Review on Computers and Software (IRECOS), Vol. 1, No. 1, July 2006, pp. 1-10.
18. R. Hoare, A. K. Jones, D. Kusic, J. Fazekas, J. Foster, S. Tung, M. McCloud, *Rapid VLIW Processor Customization For Signal Processing Applications Using Combinational Hardware Functions*, EURASIP Journal on Applied Signal Processing (JASP), Vol. 2006, Article ID 46473, 2006, pp. 1-23.
19. A. K. Jones, J. Zhang, A. Amer, *Entropy Based Evaluation of Communication Predictability in Parallel Applications*, IEICE Transactions on Information & Systems, Vol. E89-D, No. 2, February 2006, pp. 469-478.
20. X. Tang, T. Jiang, A. Jones, and P. Banerjee, *Behavioral Synthesis with power Estimation and Optimization for Unscheduled Data-Dominated Circuits*, Journal of Low Power Electronics, Vol. 1, No.3, December 2005, pp. 259-272.
21. R. Hoare, Z. Ding, S. Tung, Rami Melhem, and A. K. Jones, *A Framework for the Design, Synthesis and Cycle-Accurate Simulation of Multiprocessor Networks*, Journal of Parallel and Distributed Computing, Vol. 65, No. 10, October 2005, pp. 1237-1252.
22. Y. Yu, R. Hoare, and A. K. Jones, *A Unique Hybrid Encoding Scheme for Efficient Range Matching in Ternary Content Addressable Memory*, IEE Proceedings on Circuits, Devices & Systems - in revision.
23. Z. Ding, R. Hoare, A. K. Jones, and R. Melhem, *Level-wise Scheduling Algorithm for Fat Tree Interconnection Networks*, International Journal of Computers and Applications (IJCA) - in review since October 2006.
24. M. Baz, B. Hunsaker, G. Mehta, J. Stander, and A. K. Jones, *Mapping and Design of a Hardware Fabric*, European Journal of Operations Research (OR) - in review since April 2007, revised March 2008.

25. A. K. Jones, S. Dontharaju, L. Mats, S. Tung, J. T. Cain, P. J. Hawrylak, and M. H. Mickle, *Exploring RFID Prototyping in the Virtual Laboratory*, IEEE Transactions on Education - in revision
26. A. K. Jones, S. P. Levitan, R. A. Rutenbar, Yuan Xie, *Collaborative VLSI-CAD Instruction in the Digital Sandbox*, IEEE Transactions on Education - in revision
27. A. K. Jones, *Non-uniform "Fat Meshes" for Chip Multiprocessors*, Parallel Processing Letters, in review since May 2008.

CHAPTERS IN EDITED BOOKS

1. C. Ihrig, M. Baz, J. Stander, R. R. Hoare, B. A. Norman, O. Prokopyev, B. Hunsaker, and A. K. Jones, *Greedy Algorithms for Mapping onto a Coarse-grained Reconfigurable Fabric*, Invited Book Chapter in "Advances in Greedy Algorithms", V. Kordic, editor, I-Tech Education and Publishing, Vienna, Austria, October 2008.
2. S. Dontharaju, S. Tung, R. R. Hoare, J. T. Cain, A. K. Jones *Design Automation for RFID Tags and Systems*, Chapter 3 in "RFID Handbook: Applications, Technology, Security, and Privacy," S. Ahson and M. Ilyas, editors, Taylor and Francis, March 2008.
3. S. Tung, S. Dontharaju, L. Mats, P. J. Hawrylak, J. T. Cain, A. K. Jones, *Layers of Security for Active RFID Tags*, Chapter 33 in "RFID Handbook: Applications, Technology, Security, and Privacy." S. Ahson and M. Ilyas, editors, Taylor and Francis, March 2008.
4. A. K. Jones, S. Tung, S. Dontharaju, P. J. Hawrylak, L. Mats, J. T. Cain, *Minimum Energy/Power Considerations*, Chapter 11 in "RFID Handbook: Applications, Technology, Security, and Privacy." S. Ahson and M. Ilyas, editors, Taylor and Francis, March 2008.
5. A. Jones, D. Bagchi, S. Pal, P. Banerjee, A. Choudhary. *A Compiler with Power and Performance Optimizations*, appears in "Power Aware Computing," R. Graybill, R. Melhem, editors, Kluwer Academic Publishers, 2002.

REFEREED CONFERENCE PROCEEDINGS (FULL PAPERS)

1. S. Shao, Y. Zhang, A. K. Jones, R. Melhem, *Symbolic Expression Analysis for Compiled Communication*, IEEE Workshop on Large Scale Parallel Processing (LSPP), 2008, pp. 286.1 - 286.8.
2. S. Tung and A. K. Jones, *Physical Layer Design Automation for RFID Systems*, Reconfigurable Architecture Workshop (RAW), 2008, pp. 117.1 - 117.8.
3. G. Mehta, C. Ihrig, and A. K. Jones, *Reducing Energy by Exploring Heterogeneity in a Coarse-grain Fabric*, Reconfigurable Architecture Workshop (RAW), 2008, pp. 104.1 - 104.8.
4. Y. Yu, R. R. Hoare, and A. K. Jones, *A CAM-based Intrusion Detection System for Single-packet Attack Detection*, Reconfigurable Architecture Workshop (RAW), 2008, pp. 119.1 - 119.8.
5. A. K. Jones, S. R. Dontharaju, L. Mats, James T. Cain, and M. H. Mickle, *Exploring RFID Prototyping in the Virtual Laboratory*, MSE Conference, 2007, pp. 137-138.
6. A. K. Jones, S. Levitan, R. A. Rutenbar, and Y. Xie, *Collaborative VLSI-CAD Instruction in the Digital Sandbox*, MSE Conference, 2007, pp. 141-142.
7. A. K. Jones, R. R. Hoare, J. St. Onge, J. Lucas, S. Shao, and R. Melhem, *Linking Compilation and Visualization for Massively Parallel Programs*, IPDPS/APDCM Workshop, pp. 228.1 - 228.8, 2007.
8. C. J. Ihrig, J. Stander, and A. K. Jones, *Pipelining Tradeoffs of Massively Parallel SuperCISC Hardware Functions*, IPDPS/APDCM Workshop, pp. 227.1 - 227.8, 2007.

9. G. Mehta, J. Stander, M. Baz, B. Hunsaker, A. K. Jones, *Interconnect Customization for a Coarse-grained Reconfigurable Fabric*, IPDPS Reconfigurable Architecture Workshop (RAW), pp. 165.1 - 165.8, 2007.
10. Z. Ding, R. Hoare, A. K. Jones, R. Melhem, *Level-wise Scheduling Algorithm for Fat Tree Interconnection Networks*, Proc. of Supercomputing (SC), 2006, pp. 165.1 - 165.9.
11. R. Hoare, Z. Ding, A. K. Jones, *A Near-optimal Real-time Hardware Scheduler for Large Cardinality Crossbar Switches*, Proc. of Supercomputing (SC), 2006, pp. 164.1 - 164.12.
12. A. K. Jones, R. Hoare, S. R. Dontharaju, S. Tung, R. Sprang, J. Fazekas, J. T. Cain, and M. H. Mickle, *A Field Programmable RFID Tag and Associated Design Flow*, Proc. of the IEEE Symposium on Field Programmable and Custom Computing Machines (FCCM), 2006, pp. 165-174.
13. S. Shao, A. K. Jones, R. Melhem, *A Compiler-based Communication Analysis Approach for Multiprocessor Systems*, Proc. of IEEE/ACM International Parallel and Distributed Processing Symposium (IPDPS), 2006, DOI: 10.1109/IPDPS.2006.1639322, 10 pages.
14. Y. Yu, R. Hoare, A. K. Jones, R. Sprang, *A Hybrid Encoding Scheme that Enables Single-cycle Range Matching in Content Addressable Memory*, Proc. of IEEE International Symposium on Circuits and Systems (ISCAS), 2006, pp. 791-794.
15. A. K. Jones, R. Hoare, S. Dontharaju, S. Tung, R. Sprang, J. Fazekas, J. T. Cain, M. H. Mickle, *An Automated, FPGA-based Reconfigurable, Low-Power RFID Tag*, Proc. of IEEE/ACM Design Automation Conference (DAC), 2006, pp. 131-136.
16. R. Hoare, A. K. Jones, D. Kusic, J. Fazekas, G. Mehta, and J. Foster, *A VLIW Processor with Hardware Functions: Increasing Performance While Reducing Power*, Proc. of HPEC, September 2005, pp. 5-6.
17. K. J. Barker, A. Benner, R. Hoare, A. Hoisie, A. K. Jones, D. J. Kerbyson, D. Li, R. Melhem, R. Rajamony, E. Schenfeld, S. Shao, C. Stunkel, and P. A. Walker, *On the Feasibility of Optical Circuit Switching for High Performance Computing Systems*, IEEE/ACM Supercomputing Conference (SC), 2005, pp. 16-1 - 16-22.
18. D. Kusic, R. Hoare, A. K. Jones, J. Fazekas, J. Foster, *Extracting Speedup from C-code with Poor Instruction-level Parallelism*, Workshop of Massively Parallel Processing (WMPP), 2005, pp. 264-9 - 264-18.
19. A. K. Jones, R. Hoare, D. Kusic, J. Fazekas, and J. Foster, *An FPGA-based VLIW Processor with Custom Hardware Execution*, ACM International Symposium on Field-Programmable Gate Arrays (FPGA) 2005, pp. 107-117.
20. R. Melhem, R. Hoare, A. Jones, Z. Ding, S. Tung, D. Li, S. Shao, J. Zheng, *Enabling Predictive Multiplexed Switching in Multiprocessor Networks*, International Parallel & Distributed Processing Symposium, 2005, pp. 100-1 - 100-10.
21. X. Tang, T. Jiang, A. Jones, P. Banerjee, *Behavioral Synthesis of Data Dominated Circuits for Minimal Energy Implementation*, IEEE International Conference on VLSI Design, Taj Bengal, Kolkata, India, January 2005, pp. 267-273.
22. J. Lucas, R. Hoare, I. Kourtev, A. Jones, *LURU: Global Scope FPGA Technology Mapping with Content-Addressable Memories*, International Conference on Electronics, Circuits, and Systems (ICECS), Tel Aviv, Isreal, December, 2004, pp. 599-602.
23. A. Jones, R. Hoare, I. Kourtev, J. Fazekas, D. Kusic, J. Foster, S. Boddie, A. Muaydh, *A 64-way VLIW/SIMD FPGA Processing Architecture and Design Flow*. International Conference on Electronics, Circuits, and Systems (ICECS), Tel Aviv, Israel, December, 2004, pp. 499-502.
24. B. Brady, A. Jones, I. Kourtev, *Efficient CAD Development for Emerging Technologies using Objective-C and Cocoa*, International Conference on Electronics, Circuits, and Systems (ICECS), Tel Aviv, Israel, December 2004, pp. 369-372.

25. A. Jones, X. Tang, P. Banerjee, *Compile-time Simulation for Low-Power Optimization using SystemC*, Modelling and Simulation Conference, Marina Del Ray, CA, 2004, pp. 78-83.
26. T. Jiang, X. Tang, A. Jones, P. Banerjee, *Optimizing Power While Exploiting Fine Grain Parallelism on FPGAs*, IASTED International Conference on Parallel and Distributed Computing and Systems (PDCS), November 2003, pp. 357-362.
27. R. Mukherjee, A. Jones, P. Banerjee, *System Level Synthesis of Multiple IP Blocks in the Behavioral Synthesis Tool*, International Conference on Parallel and Distributed Computing and Systems (PDCS), November 2003, pp.363-368. *Best Paper Award Nominee*
28. X. Tang, T. Jiang, A. Jones, P. Banerjee, *Compiler Optimizations in the PACT HDL Behavioral Synthesis Tool for ASICs and FPGAs*, IEEE International SoC Conference (SoC), September 2003, pp. 189-192.
29. A. Jones, D. Bagchi, S. Pal, X. Tang, A. Choudhary, P. Banerjee, *PACT HDL: A C Compiler with Power and Performance Optimizations*, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), Grenoble, France, October 2002, pp. 188-197.
30. A. Jones, A. Nayak, P. Banerjee. *Parallel Implementation of Matrix and Signal Processing Libraries on FPGAs*, International Conference on Parallel and Distributed Computing and Systems (PDCS), Anaheim, CA, August 2001, pp. 370-377. *Best Paper Award Nominee*
31. P. Banerjee, N. Shenoy, A. Choudhary, S. Hauck, C. Bachmann, M. Chang, M. Haldar, P. Joisha, A. Jones, A. Kanhare, A. Nayak, S. Periyacheri, M. Walkden, *MATCH: A MATLAB Compilation Environment for Configurable Computing Systems*, International Symposium on Field-Programmable Custom Computing Machines (FCCM), Napa, CA, 2000, pp. 39-48.
32. S. Periyacheri, A. Jones, A. Nayak, D. Zaretsky, P. Banerjee, N. Shenoy, A. Choudhary. *Library Functions in Reconfigurable Hardware for Matrix and Signal Processing Operations in MATLAB*, International Conference on Parallel and Distributed Computing and Systems (PDCS 1999), Cambridge, MA, November, 1999.

REFEREED CONFERENCE PROCEEDINGS (EXTENDED ABSTRACTS)

1. J. Lucas, R. Hoare, I. Kourtev, and A. K. Jones, *Technology Mapping for Field Programmable Gate Arrays using Content-Addressable Memory (CAM)*, Proc. of the IEEE Symposium on Field Programmable and Custom Computing Machines (FCCM), 2006, pp. 299-300.
2. G. Mehta, R. Hoare, J. Stander, A. K. Jones, *A Low-Energy Reconfigurable Fabric for the SuperCISC Architecture*, Proc. of the IEEE Symposium on Field Programmable and Custom Computing Machines (FCCM), pp. 309-310.
3. G. Mehta, R. Hoare, J. Stander, A. Jones, *Design Space Exploration for Low-Power Reconfigurable Fabrics*, Proc. of IEEE/ACM Reconfigurable Architectures Workshop (RAW), 2006.
4. R. Hoare, A. K. Jones, D. Kusic, J. Fazekas, G. Mehta, and J. Foster, *A VLIW Processor with Hardware Functions: Increasing Performance While Reducing Power*, Proc. of the Workshop on High Performance Embedded Computing (HPEC'05).
5. J. Lucas, R. Hoare, I. Kourtev, and A. K. Jones, *LURU2: Optimizing Technology Mapping for FPGAs Using CAMs*, IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), 2005, pp. 293-294.
6. R. Mukherjee, A. Jones, P. Banerjee, *Handling Data Streams while Compiling C Programs onto Hardware*, International Symposium on VLSI (ISVLSI), Lafayette, Louisiana, February, 2004, pp. 271-272.
7. A. Jones, P. Banerjee, *An Automated and Power-Aware Framework for Utilization of IP Cores in Hardware Generated from C Descriptions Targeting FPGAs*, IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), Napa, CA, 2003, pp.284-285.

8. A. Jones, P. Banerjee, *An Automated and Power-Aware Framework for Utilization of IP Cores in Hardware Generated from C Descriptions Targeting FPGAs*, ACM International Symposium on Field-Programmable Gate Arrays (FPGA), Monterey, California, February, 2003, pp. 244.

TECHNICAL REPORTS AND POPULAR JOURNALS

1. B. Brady, A. Jones, I. Kourtev, *Rapid CAD Prototyping for Nanotechnology using Objective-C and Cocoa*, University of Pittsburgh ECE Department Technical Report: TR-ECE-2004-04-001, April, 2004.
2. X. Tang, T. Jiang, A. K. Jones, P. Banerjee, *Behavioral Synthesis with Power Estimation and Optimization for Unscheduled Data-Dominated Circuits*, Center for Parallel and Distributed Computing Technical Report: CPDC-TR-2004-03-001, March, 2004.
3. A. Jones, P. Banerjee, *An Automated and Power-Aware Framework for Utilization of IP Cores in Hardware Generated from C Descriptions*, Center for Parallel and Distributed Computing Technical Report: CPDC-TR-2002-04-02, Northwestern University, April, 2002.
4. A. Jones, D. Bagchi, S. Pal, X. Tang, A. Choudhary, P. Banerjee, *PACT HDL: A C Compiler Targeting ASICs and FPGAs with Power and Performance Optimizations*, Center for Parallel and Distributed Computing Technical Report: CPDC-TR-2002-03-01, Northwestern University, March, 2002.
5. D. Bagchi, S. Pal, A. Jones, A. Choudhary, P. Banerjee, *Pipelining Memory Accesses on FPGAs for Image Processing Algorithms*, Center for Parallel and Distributed Computing Technical Report: CPDC-TR-2001-12-002, Northwestern University, December, 2001.
6. P. Banerjee, N. Shenoy, A. Choudhary, S. Hauck, C. Bachmann, M. Chang, M. Haldar, P. Joisha, A. Jones, A. Kanhare, A. Nayak, S. Periyacheri, M. Walkden, *MATCH: A MATLAB Compiler for Configurable Computing Systems*, Center for Parallel and Distributed Computing Technical Report: CPDC-TR-9908-013, Northwestern University, September, 1999.

INVITED PRESENTATIONS AND WORKSHOPS

- Virginia Tech** *Low-energy Reconfigurable Computing*, Presentation, November 9th, 2007.
- Westinghouse, Inc.** *Hardware Devices and Electronic Design Automation*, Presentation, August, 6th 2004.
- Northrup Grumman, Corp.** *The Data Forest Supercomputer*, Presentation, April 21st, 2004.
- Illinois Institute of Technology** *PACT HDL: A C Compiler Targeting ASICs and FPGAs with Power and Performance Optimizations*, Presentation, March 5th, 2003.
- University of Tennessee** *PACT HDL: A Compiler Targeting ASICs and FPGAs with Power and Performance Optimizations*, Presentation, March, 2003.

GRANTS

CURRENT

- National Science Foundation** *NSF CAREER: Compiled Communication for Chip Multiprocessors*, A. K. Jones (PI), \$400,000, 01/01/2009 - 12/31/2013 - pending.
- The Technology Collaborative** *Computer Engineering Laboratory Upgrade*, PI with S. Levitan, \$75,000, 07/01/07 - 06/30/10.

National Science Foundation *NSF Foundations of Computing Processes and Artifacts: Enabling Circuit Switching with Compiler and Runtime Analysis for High Performance Systems*, PI with R. Melhem, \$325,000, 05/01/2007 - 04/30/2010.

The Technology Collaborative *Hardware Fabrics: Embedded Solutions for High Performance and Micro Power.*, \$298,070, 03/01/2007 - 02/28/2009.

Synplicity, Inc. *FPGA and ASIC Computer Aided Design Tools Donation*, Fair Market Value \$57,772,500, 07/01/2004 - 06/30/2009.

COMPLETED

Swanson Institute for Technical Excellence *An Ultra Low-power, Gen 2 Compatible Active RFID Tag*, \$39,800, PI with M. H. Mickle, J. T. Cain, J. Rajgopal, and B. A. Norman, 08/01/2006 - 07/31/2007.

Swanson Institute for Technical Excellence *Optimizing Antenna/Reader Placement for Arbitrary Orientations of Passive RFID Tags*, \$39,800, Co-PI with J. Rajgopal (PI), B. A. Norman, M. H. Mickle, and J. T. Cain, 08/01/2006 - 07/31/2007.

University of Pittsburgh *A Low-Energy Computing Fabric with Design Flow*, \$37,106, 07/01/2006 - 06/31/2007.

The Technology Collaborative *Electronic Design Education Program Digital Sandbox Course Collaboration*, \$27,330, PI, 08/01/2006-12/31/2006.

National Instruments *National Instruments Equipment Grant Proposal*, \$50,000, Co-PI, with M. H. Mickle (PI), and J. T. Cain.

The Technology Collaborative *SECuRFID: Secure, Efficient, Customizable RFID Systems*, \$30,000, PI with M. H. Mickle and J. T. Cain, 07/01/2006 - 12/31/2006.

Tego, Inc. *RF Front-End Integration and Testing with Atlas*, \$59,000, Co-PI with M. H. Mickle (PI), and J. T. Cain, 8/1/2006 - 12/31/2006.

The Technology Collaborative *Enabling a Low-power, Secure RFID Tag*, PaCSCI Phase I Grant, \$10,049, 10/1/2005 - 06/30/2006.

Xilinx, Inc. *XUP Software Donation for FPGA and Embedded Computing Development for Research and Teaching Labs, 200 seats*, Fair Market Value \$3,735,000, 05/25/05.

ADCUS, Inc. *Development Tools and Microprocessor Development System*, Fair Market Value \$400,000, Co-PI, with J. T. Cain, R. Hoare, and M. Mickle (PI).

IBM/DARPA *Productive, Easy to use, Reliable Computer Systems, High Productivity Computing Systems (HPCS) - Phase II*, \$900,000, 09/01/03 - 08/31/06, Co-PI, with R. Melhem (PI), A. Amer, R. Hoare.

Pittsburgh Digital Greenhouse *Digital Sandbox Maintenance Grant*, \$75,000, 07/01/04 - 06/30/05, Co-PI with T. Cain, I. Kourtev, S. Levitan, R. Hoelzeman.

ADCUS, Inc. *An RFID Tag Generation System for the ADCUS EISC 16 Bit Processor and Design Environment*, \$175,947, 09/01/04 - 08/31/05, Co-PI, with M. Mickle (PI), T. Cain, and R. Hoare.

Swanson Center for Micro and Nano Systems *Efficient, Low-Power Computing for Micro and Nano Systems: Exploiting Different Forms of Parallelism*, \$30800, 08/01/04 - 07/31/05, PI, with R. Hoare.

Xilinx, Inc. *XUP Software Donation*, Fair Market Value \$18,675, 10/01/04 - 09/30/04.

COURSES TAUGHT

UNIVERSITY OF PITTSBURGH

- ECE 2120 Hardware Design Methodologies** – Introduction to hardware design methodologies through use of industry tools. Students use design automation tools to design, simulate, and synthesize designs for ASICs and FPGAs using hardware description languages (e.g. VHDL, Verilog, and/or SystemC). Techniques for design optimization, simulation, and synthesis of combinatorial functions, data paths, and finite state machines are covered in depth.
- ECE 2130(3131) VLSI-CAD** – Introduction to the fundamental concepts to building computer-aided design tools for VLSI. Topics include fundamental data structures including cubes and BDDs, algorithms for logic minimization, placement and routing of standard cells, verification, etc. Students complete homework assignments, and programming projects.
- ECE 2140 System-on-a-Chip Design (SoC)** – Students learn fundamental concepts of building an SoC. Topics include hardware and software partitioning, design and reuse of intellectual property blocks, design specification. All students work on different components of a term long SoC design targeted for actual hardware (typically an FPGA containing embedded hard core processor(s)). The students are tasked with making progress report presentations, communication between groups, creating interface specifications. Appropriate papers and homeworks are assigned.
- ECE/CoE 0501 Digital Systems Laboratory (course director)** – A sequence of laboratory assignments to reinforce material from EE/CoE 0132 through building of combination and sequential circuits eventually building a simple datapath with register file and ALU. Students learn to use a breadboard, Oscilloscope, Logic Analyzer, a schematic editor, and FPGA.
- ECE/CoE 0132 Digital System Design** – Introduction to the fundamentals of digital systems and design including logic gates, boolean algebra, karnaugh maps, transistor schematics, flip-flops, and finite state machines.

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- ECE 397 Introduction to ASIC and FPGA Design** – Introduction to the process of designing application specific hardware implementations of algorithms for ASICs and FPGAs. Students work with commercial high-level synthesis tools and hardware description languages to realize these designs. Topics covered include register transfer level design, finite state machines, design reuse and intellectual property cores, and memory pipelining.
- ECE 203 Introduction to Computer Engineering** – Provides an introduction to computer engineering concepts, both hardware and software, with emphasis placed on digital logic concepts. Topics include binary number representations, Boolean algebra, simplification methods for combinational circuits, introduction to sequential circuits, introduction to assembly language programming, and networks. The concepts are applied to a hands-on laboratory assignments that includes hardware and software designs of a controller to navigate a robot through a given obstacle course.
- ECE 303 Advanced Digital Design** – Advanced topics in digital design from two-level to multi-level combinational logic, finite state machine design, minimization, and synthesis. Introduction of contemporary computer-aided design (CAD) tool theory and use for optimization. Introduction of hardware description languages for combinational and sequential circuits.
- ECE 361 Computer Architecture** – Teaches the design of a complete computer system. Design topics include instruction set architectures, datapaths, control, memory hierarchies such as main memory, caches and virtual memory, and I/O systems. Students work with commercial CAD tools to design a simple ALU and single cycle processor covering these topics.

ECE 358 Introduction to Parallel Computing – Provides an introduction to the field of parallel computing. Includes an overview of three basic parallel computing paradigms: shared memory, distributed memory message passing, and data parallel computing. These concepts are reinforced with hands-on experience with real parallel programming on actual parallel machines.

STUDENT
SUPERVISION

DOCTORAL DISSERTATIONS SUPERVISED

Ying Yu, Ph.D. A Content-Addressable Memory Assisted Intrusion Prevention Expert System for Gigabit Networks – now at Marvell Semiconductor.

Swapna R. Dontharaju, Ph.D. Design Automation for Low Power RFID Tags – now at Intel.

Shenchih Tung, Ph.D. An Architectural Approach for Reducing Power and Increasing Security of RFID Tags – joining Concurrent EDA, LLC.

Mustafa Baz – Ph.D. Optimization of Mapping onto a Flexible Low-power Electronic Fabric Architecture – now with Applied Decision Technologies, Inc. – *Co-Advised with Brady Hunsaker*.

MASTERS THESES SUPERVISED

Colin J. Ihrig, M.Sc. Static Timing Analysis Based Transformations of Super-Complex Instruction Set Hardware Functions – now a Ph.D. student.

Gerold Joseph Dhanabalan, M.Sc. A Physical Implementation of a Reconfigurable Hardware Fabric with Low Power Extensions – now the Texas Instruments.

Justin Stander, M.Sc. Electronic Design Automation for an Energy-Efficient Coarse-Grain Reconfigurable Fabric Architecture – now with Concurrent, EDA, LLC.

Joshua M. Lucas, M.Sc. Technology Mapping for Circuit Optimization using Content-Addressable Memory – now with Lockheed Martin.

Joshua Fazekas, M.Sc. The VLIW-SuperCISC Compiler: Exploiting Parallelism from C Code Applications.

Salman Arif, M.Sc. (Professional) – now with Sun Microsystems.

Rajarshi Mukherjee, M.Sc. (with Prith Banerjee)

CURRENT STUDENT SUPERVISION

Gayatri Mehta – Ph.D. candidate (Architectures for Reconfigurable Fabrics), expected Summer 2008.

Shuyi Shao – Ph.D. candidate (Compilers for Predicting Communication in Parallel Networks), expected Summer 2008. – *Co-Advisor with Rami Melhem*

Colin Ihrig – Ph.D. student (Technology Dependent Delay Elements and Pipelining)

Vyasa Sai – Ph.D. student (Compilers for multi-core computing)

Yu Zhang – M.Sc. student (Behavioral Synthesis of Image, Signal Processing, Networking, and Security Applications)

Hariram Ravindran – M.Sc. student (Low-power data centers)

Alicia Beacom – B.Sc. student (Power macromodeling of various bitwidth datapaths for RFID synthesis)

STUDENT THESIS COMMITTEES

University of Pittsburgh: Department of Electrical and Computer Engineering: (Ph.D) Xiuyi Zhou, Gayatri Mehta, Shenchih Tung, Swapna Dontharaju, Shuyi Shao, Zhu Ding, Ying Yu, Baris Taskin, Rob Murawski, Joe Hines(M.Sc.): Gerold Joseph Dhanabalan, Colin Ihrig, Justin Stander, Jeff Schuster, Johnny Ng, Josh Lucas, Joseph St. Onge, Josh Fazekas, Katrina Werger, Peter Hawrylak, Jake Repanshek, Josh Lucas, Dara Kusic, Kshitij Gupta.

University of Pittsburgh: Department of Computer Science: (Ph.D.) Yuqiang Huang, Shuyi Shao, David Essary.

Northwestern University: Department of Electrical and Computer Engineering: (M.Sc.): Rajarshi Mukherjee

PROFESSIONAL SERVICE

EDITORIAL SERVICE

Associate Editor, special issue, TRETTS: ACM Transactions on Reconfigurable Technology and Systems, special issue on Special Issue on Security in Reconfigurable Systems Design.

Associate Editor, special issue, PPL: Parallel Processing Letters, special issue on the Workshop for Large Scale Parallel Processing.

Associate Editor, special issue, TODAES: ACM Transactions on Design Automation of Electronic Systems, special issue on Demonstrable Hardware and Software Systems II.

Associate Editor, JOLPE: Journal of Low Power Electronics, 2007 - *current*.

Associate Editor, IJCA: IASTED International Journal of Computers and Applications, 2004 - *current*.

Associate Editor, RPEE: Recent Patents in Electrical Engineering, 2007 - *current*.

CONFERENCE COMMITTEES

University Booth, DAC: University Booth Coordinator, Design Automation Conference, 2005 - 2006. SIGDA Advisor, 2006 - *current*

Program Chair, MSE: Microelectronic Systems Education Conference, 2009.

Program Committee, DAC Ph.D. Forum Program Committee, Publicity Chair, DAC Ph.D. Forum, 2008 - *current*.

Steering Committee, WLSPP Steering Committee, Workshop on Large-Scale Parallel Processing at the International Parallel & Distributed Processing Symposium, 2008 - *current*. *Publicity chair*, 2008.

Organizing Committee, Special Session in MPP at ADPCM/IPDPS: Organizing Committee, Special Session in Massively Parallel Processing at the Workshop on Advances in Parallel and Distributed Computing Models (ADPCM) at the International Parallel & Distributed Processing Symposium, 2007.

Program Committee, MSE: Program Committee, Microelectronic System Education Conference, 2005 - *current*.

Program Committee, WMPP: Program Committee, Workshop on Massively Parallel Processing, 2005.

Technical Committee, ICPP: Technical Committee, International Conference on Parallel Processing, 2005 - *current*.

Technical Committee, PDCS: Technical Committee, IASTED Parallel and Distributed Computing and Systems Conference, 2003-2005, 2007 - *current*.

PROFESSIONAL SOCIETY MEMBERSHIPS

Senior Member, IEEE/IEEE Computer Society

Association for Computing Machinery (ACM)

Special Interest Group in Design Automation (SIGDA) – **Executive Committee Member**

International Association of Science and Technology for Development (IASTED)

REVIEWER

IEEE Transactions on VLSI

IEEE Transactions on CAD

IEEE Transactions on Automation Science and Engineering

ACM Transactions on Embedded Computing Systems

ACM Transactions on Reconfigurable Technology and Systems

Design Automation Conference (DAC)

Academic Press Journal of Parallel and Distributed Computing

Asia and South Pacific Design Automation Conference

IASTED Parallel and Distributed Computing and Systems Conference

MSE Conference