

## **ABSTRACT**

### **APPLICATION-SPECIFIC ARCHITECTURE FRAMEWORK FOR HIGH-PERFORMANCE LOW-POWER EMBEDDED COMPUTING**

**by**

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The design space of embedded systems is enormously large. These embedded applications have strict requirements on power consumption, performance, cost, and time to market. It is extremely critical to fully address these constraints when designing microprocessors for embedded systems.

This dissertation proposes Framework-based Instruction-set Tuning Synthesis (FITS). FITS is an architectural and microarchitectural innovation that effectively tackles all the above requirements. FITS reduces power consumption by running applications with half the code size and much improved locality, which allows the use of a smaller instruction cache that achieves higher hit rates while requiring less power to operate.

FITS improves the performance through custom-tailored application-specific instruction set architecture (ISA) and ground-breaking microarchitectural enhancement. The application-specific instruction set tailoring is achieved by synthesizing ISA to match precisely the requirements of the targeted application. The microarchitecture is

enhanced by integrating the revolutionary Versatile Integrated Processing (VIP) unit and a Zero-Overhead Loop Execution (ZOLE) unit into it. The VIP unit is a universal data-crunching engine that delivers superior data computing and data streaming performances. The ZOLE unit streamlines the program control flow by removing expensive loop control overhead from both nested and non-nested loops. Both architectural and microarchitectural innovations are accomplished by replacing the fixed instruction decoder of general-purpose embedded processors with a programmable decoder. Using a programmable decoder decouples the microarchitecture from the ISA so that designers can add new capabilities to the microarchitecture without being restricted by the limited instruction space.

A general-purpose, fully-capable microarchitecture reduces the design cost and shortens the time to market by leveraging fabrication advantages of a single-chip solution that can amortize high non-recurring engineering cost and long turnaround design cycle through mass production.

Through the use of a programmable decoder, and an enhanced general-purpose microarchitecture equipped with VIP and ZOLE, FITS pioneers a new genre of embedded microprocessors that can achieve application-specific processor performance and low energy consumption, while maintaining the fabrication advantages of a mass-produced single-chip solution that yields low production cost and fast time to market.