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RESEARCH INTERESTS

Processor microarchitecture: chip multiprocessors, 3D chips, cache management, power and thermal management, interconnection, performance optimization.
Embedded systems: energy conservation, network processors, sensor networks.
Hardware security: architecture support for secure software execution.

EDUCATION

Ph.D. in Computer Science, University of Arizona, September 2002; Advisor: Rajiv Gupta
M.S. in Computer Science, University of Pittsburgh, June 1999; Advisor: Rami Melhem
M.A. in Applied Mathematics, Worcester Polytechnic Institute, August 1997; Advisor: Dalin Tang
B.S. in Computer Science, Nanjing University, P. R. China, June 1995.

PROFESSIONAL POSITIONS HELD

Associate Professor, Department of Electrical and Computer Engineering, University of Pittsburgh, September 2009 – present.
Assistant Professor, Department of Electrical and Computer Engineering, University of Pittsburgh, September 2006 – August 2009.
Assistant Professor, Department of Computer Science and Engineering, University of California, Riverside, September 2002 – August 2006.

AWARDS

Best Paper Nominee, The 15th International Symposium on High-Performance Computer Architecture 2009
NSF Faculty Early Career Development Award (CAREER) 2008
Best Paper, International Conference on Computer Design, processor architecture track 2007
Regent's Faculty Fellowship / Faculty Development Award, UC Riverside 2003, 2004

EXTERNALLY FUNDED RESEARCH PROPOSALS

Intel Corporation, PI, *Towards Low-Power System-on-Chip*, \$50,000, November, 2008 – October, 2009.
Abstract: A system-on-chip (SoC) may contain combinations of cores of different functions such as microprocessors, memories, a/v controllers, modem, 2D and 3D graphics controllers, DSP functions etc. The high integration of vastly different function cores on-chip with the continuous technology shrinking brings forth the challenges in low power SoC designs. SoCs are widely used in consumer electronics, mobile internet devices, and embedded markets. Most of them are battery powered. An energy-efficient design can not only extend the battery life, but also allow for higher performance and higher integration of more IP blocks on-chip. In this proposal, we put forward a suite of techniques to tackle the critical factors of the power consumption of an SoC, namely the switching activity of different IP blocks, the voltage and frequency of them, and the leakage power of the memory modules.

National Science Foundation, PI, *CAREER: Thermal-Aware Task Scheduling for Embedded Planar and 3D Chip Multiprocessors*, CNS-0747242, \$400,000, 9/1/2008-8/31/2013.

Abstract: This CAREER project proposes innovative solutions to tackle the thermal problems for modern compact embedded systems including 2D or 3D multicore processors that support powerful

and versatile applications. The objective of this proposal is to develop proactive thermal management techniques which prevent the temperature from increasing above the threshold and avoid performance throttling. This is in contrast to traditional techniques which only react to thermal violations by enforcing performance throttling to cool down the processor. The proposed techniques leverage the natural discrepancies in thermal behavior among different applications, and schedule them among multiple cores to keep the chip temperature within a given budget. The mission of such scheduling is to minimize thermal violations across all cores on-chip, improve the performance, and diminish overheating-induced problems such as reduced reliability, low circuit speed, and high leakage power.

National Science Foundation, PI (Co-PI: Youtao Zhang), *An Update-Conscious Compilation Framework for Energy-Efficient Code Dissemination in Wireless Sensor Networks*, CNS-0720595, \$120,000, 9/1/2007-8/31/2009.

Abstract: Wireless sensor networks (WSN) often require code changes, such as software patches, new functions etc. A naïve way of performing code changes in a WSN is to send the code or code differences in form of data packets, and let the sensor nodes compute the new code. Since energy consumed by data transmission is much higher than that consumed by local instruction execution, it is important to be energy-efficient during the code dissemination in WSNs. This project proposes update-conscious compilation for achieving energy-efficient code dissemination. The integrated compilation framework consists of a set of sink-side update-aware compilation techniques, and a sensor-side software-decoder/binary-rewriter. Specifically, the intellectual merits of this project are: 1) update-aware register allocation techniques; 2) update-aware data allocation techniques; 3) update-aware code placement techniques; 4) tools for enabling update-aware compilation. Through this research, we are committed to cultivating a strong interest and a positive attitude among students towards embedded software development.

National Science Foundation, PI (Co-PIs: Sheldon Tan, Jie Chen), *Fast Software Thermal Sensing and Control for Efficient Dynamic Thermal Management*, CCF-0734339, \$275,000, 4/1/2006-3/31/2009.

Abstract: This proposal addresses the fundamental challenges in today's on-chip thermal sensing and control problems. The thermal sensing technique in even the most recent processors predominantly relies on thermal diodes or sensors. Both suffer from the fixed-location problem as on-chip hot spots migrate at run time. This project aims to develop novel techniques for spectrum and high precision temperature sensing to mitigate this problem. The proposed solutions can lead to more efficient and effective on-line thermal management. The intellectual merit of the project includes the development of a fast, lean, and accurate software thermal sensor for online temperature tracking. The software adopts a highly efficient and fine-tuned numerical method to calculate temperatures at a fine granularity both temporally and spatially. Experimentation will demonstrate its superior accuracy and speed, and hence the great potential of becoming a truly competitive remedy for chip temperature sensing.

National Science Foundation, PI (PI of collaboration institute: Youtao Zhang), *Collaborative Research: Architectural Support for Security and Privacy Protection on Uni- and Multi- Processors*, CCF-0430021, \$80,001 (UCR funds: \$54,001), 11/1/2004-10/31/2006.

Abstract: Software programs executing on a broad range of internet systems are constantly subject to malicious attacks in various forms. Program execution behavior might be altered causing substantial damage, data may become corrupted and privacy can be greatly compromised. This proposal develops a secure processor model which secure applications can easily be built on. We augment the existing microprocessor architecture to incorporate new features. The proposed architectural components address a broad range of attacks on uniprocessor and multiprocessor architectures. In particular, we develop novel architecture support for enhancing uniprocessor security. The confidentiality and integrity of such a microarchitecture are maintained through encryption and decryption of the code and data transferred across the chip. While the efficiency of encryption has been solved successfully by PIs and others, the computation intensive nature of crypto operations has led the verification of inbound traffic being delayed. This project also designs a strong verification engine with which information leakage of on-chip

data is prevented. This was a collaborative project with University of Texas, Dallas. The PI there was Professor Youtao Zhang.

National Science Foundation, Senior Personnel (PI: Laxmi Bhuyan, co-PI: Walid Najjar, Gianfranco Ciardo), *MRI: Acquisition of an Ultra Low-Latency Multiprocessor System with On-Board Hardware Accelerators*, CNS-0619223, \$330,000, 8/15/2006-7/31/2008.

Abstract: This project, acquiring an extremely low-latency multiprocessor system with on-board hardware accelerators, develops efficient scalable algorithms and software resource management schemes for individual applications. The cluster is used in support of the following projects. 1) Investigation into scalable hardware and software design for Internet web servers and data centers; 2) Symbolic model checking; 3) Pattern discovery for biological applications; 4) Automatic compilation of high-level code, such as C or Fortran, into RTL VHDL code; 5) Warp processing; and 6) Augmenting existing microarchitecture with security protections ensuring integrity & confidentiality of program execution. The proposed cluster can be partitioned into several subclusters that can work independently and simultaneously on different applications, provides ultra low message passing latency within a sub-cluster and between sub-clusters, and provides an SMP environment with processors that can be used for tightly-coupled codes; thus a hybrid programming model suits different applications. The research projects on FPGA compilation, hardware/software partitioning, and CPU micro architecture design require an FPGA-based system for a test bed.

STUDENT ADVISING

GRADUATED PH.D. STUDENTS

1. Yan Luo
Ph.D. in Computer Science and Engineering, 2005, University of California Riverside
Performance Evaluation and Low Power Design of Network Processors
co-advised with Laxmi Bhuyan (UC Riverside) Jan. 2003 – Aug. 2005
Source of support: NSF grants and TAship
First employment: Assistant Professor, University of Massachusetts Lowell, MA.
2. Lingling Jin
Ph.D. in Computer Science and Engineering, 2006, University of California Riverside
Software Thermal Monitoring and Management for High-Performance Microprocessors
Major advisor, Sept. 2002 – Aug. 2006
Source of support: NSF grants, UCR startup fund, and TAship
First employment: nVidia Corp., CA.
3. Lan Gao
Ph.D. in Computer Science and Engineering, 2007, University of California Riverside
Security Designs for Uni and Multi- Processors
Major advisor, Sept. 2002 – Aug. 2006; co-advised with Marek Chrobak Sept. 2006 – Aug. 2007
Source of support: NSF grants, UCR startup fund, and TAship
First employment: VMware Corp., CA.
4. Jia Yu
Ph.D. in Computer Science and Engineering, 2007, University of California Riverside
Architectural and Compiler Optimization for Network Processors
Major advisor, Sept. 2002 – Aug. 2006; co-advised with Laxmi Bhuyan Sept. 2006 – Aug. 2007
Source of support: NSF grants, UCR startup fund and TAship
First employment: VMware Corp., CA.
5. Wei Wu
Ph.D. in Computer Science and Engineering, 2008, University of California Riverside
Power/Thermal Modeling and Dynamic Thermal Management for SRAM Structure

Major advisor, Jan. 2004 – Aug. 2006; co-advised with Sheldon X.-D. Tan Sept. 2006 – Jan. 2008
Source of support: NSF grants and TAsip
First employment: Intel Hillsboro, OR.

GRADUATED M.S. STUDENTS

1. Jiannan Wang
M.S. in Computer Science and Engineering, 2003, University of California Riverside
An Implementation of Zero Value Based Address Correlation
Major advisor, Sept. 2002 – Dec. 2003
Source of support: UCR TAsip

CURRENT STUDENTS

1. Xiuyi Zhou
Ph.D. program, Electrical and Computer Engineering Dept., University of Pittsburgh
Major advisor, Sept. 2006 – present
Passed preliminary (Dec. 2007) and comprehensive (Feb. 2008) exams
Expected graduation time: Summer 2010
Source of support: University of Pittsburgh startup fund
2. Lin Li
M.S. program with intent for Ph.D., Electrical and Computer Engineering Dept., University of Pittsburgh
Major advisor, Sept. 2007 – present
Source of support: NSF grant and TAsip
3. Yi Xu
Ph.D. program, Electrical and Computer Engineering Dept., University of Pittsburgh
Major advisor, Sept. 2007 – present
Passed preliminary (Dec. 2008) and comprehensive (Feb. 2009) exams
Source of support: NSF grant and TAsip
4. Ping Zhou
Ph.D. program, Electrical and Computer Engineering Dept., University of Pittsburgh
Major advisor, Jan. 2008 – present
Source of support: NSF grant and TAsip
5. Bo Zhao
Ph.D. program, Electrical and Computer Engineering Dept., University of Pittsburgh
Major advisor, Sept. 2007 – present
Source of support: NSF grant and TAsip
6. Lei Jiang
Ph.D. program, Electrical and Computer Engineering Dept., University of Pittsburgh
Major advisor, Sept. 2009 – present
Source of support: TAsip
7. Liang Liao
M. S. program, Electrical and Computer Engineering Dept., University of Pittsburgh
Major advisor, Sept. 2008 – present
Source of support: None
8. Yu Du
Ph.D. program, Computer Science Dept. University of Pittsburgh
co-advised with Youtao Zhang, Sept. 2006 – present
Source of support: NSF grant and TAsip

REFEREED PUBLICATIONS

JOURNALS

- [1] Weijia Li, Youtao Zhang, Jun Yang, Jian Zheng, "Towards Update-Conscious Compilation for Energy-Efficient Code Dissemination in WSNs," *to appear, ACM Transactions on Architecture and Code Optimization*, 2009.
- [2] Dinesh Suresh, Banit Agrawal, Jun Yang, Walid Najjar, "Tunable and Energy Efficient Bus Encoding Techniques," *IEEE Transactions on Computers*, Vol. 58, No. 8, pp. 1049-1062, 2009.
- [3] Xiuyi Zhou, Jun Yang, Yi Xu, Youtao Zhang, Jianhua Zhao, "Thermal-aware Task Scheduling for 3D Multi-core Processors," *to appear, IEEE Transactions on Parallel and Distributed Systems*, 2009.
- [4] Dinesh Suresh, Banit Agrawal, Jun Yang, Walid Najjar, "Energy-Efficient Encoding Techniques for Off-Chip Data Buses," *ACM Transactions on Embedded Computing Systems*, Vol. 8, Iss. 2, Article 9, January 2009.
- [5] Youtao Zhang, Jun Yang, Lan Gao, "Supporting Flexible Streaming Media Protection through Privacy-aware Secure Processors," *Journal of Computers and Electrical Engineering, Elsevier, Special Issue on Circuits and Systems for Real-Time Security and Copyright Protection of Multimedia*, Vol. 35, Iss. 2, pp. 286-299, March 2009.
- [6] Youtao Zhang, Jun Yang, Hai Vu, Yizhi Wu, "The Design and Evaluation of Interleaved Authentication for Filtering False Reports in Multipath Routing WSNs," *Wireless Networks, The Journal of Mobile Communication, Computation and Information*, Springer Netherlands, DOI: 10.1007/s11276-008-0199-0, May 2008.
- [7] Wei Wu, Lingling Jin, Jun Yang, Pu Liu, Sheldon X.-D. Tan, "Efficient Power Modeling and Soft-ware Thermal Sensing for Runtime Temperature Monitoring," *ACM Transactions on Design Automation of Electronic Systems, Special Issue on Demonstrable Software Systems and Hardware Platforms*, Vol. 12, Iss. 3, Article No. 26 (29 pages), August 2007.
- [8] Yan Luo, Jia Yu, Jun Yang, Laxmi Bhuyan, "Conserving Network Processor Power Consumption by Exploiting Traffic Variability," *ACM Transactions on Architecture and Code Optimization*, Vol. 4, Iss. 1, Article No. 4 (26 pages), March 2007.
- [9] Pu Liu, Hang Li, Lingling Jin, Wei Wu, Sheldon X.-D. Tan, Jun Yang, "Fast Thermal Simulation for Runtime Temperature Tracking and Management," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 12, pp. 2882-2894, December 2006.
- [10] Chuanjun Zhang, Frank Vahid, Jun Yang, Walid Najjar, "A Way-Halting Cache for Low-Energy High-Performance Systems," *ACM Transactions on Architecture and Code Optimization*, Vol. 2, Iss. 1, pp. 34-54, March 2005. (27 citations)
- [11] Jun Yang, Lan Gao, Youtao Zhang, "Improving Memory Encryption Performance in Secure Processors," *IEEE Transactions on Computers*, Vol. 54, No. 5, pp. 630-340, May 2005.
 - Featured in MIT Technology Review, July 2005.
- [12] Jun Yang, Jia Yu, Youtao Zhang, "A Low Energy Cache Design for Multimedia Applications Exploiting Set Access Locality," *Journal of Systems Architecture: the EUROMICRO Journal*, Vol. 51, Iss. 10-11, pp.653-664, October/November 2005, Elsevier North-Holland Inc.
- [13] Youtao Zhang, Jun Yang, "Reducing I-cache Energy of Multimedia Applications through Low Cost Tag Comparison Elimination," *Journal of Embedded Computing*, Vol. 1, Iss. 4, pp. 461-470, December 2005, IOS Press, Amsterdam, The Netherlands.
- [14] Jun Yang, Rajiv Gupta, Chuanjun Zhang, "Frequent Value Encoding for Low Power Data Buses," *ACM Transactions on Design Automation of Electronic Systems*, Vol. 9, Iss. 3, pp. 354-384, July 2004.

- [15] Jun Yang, Rajiv Gupta, "Frequent Value Locality and Its Applications," *ACM Transactions on Embedded Computing Systems (inaugural issue)*, Vol. 1, Iss. 1, pp. 79-105, November 2002. (38 citations)
- [16] Dalin Tang, Jun Yang, "A Free Moving Boundary Model and Boundary Iteration Method for Unsteady Viscous Flow in Stenotic Elastic Tubes," *SIAM Journal on Scientific Computing*, Vol. 21, No. 4, pp. 1370-1386, 2000.
- [17] Dalin Tang, Jun Yang, Chun Yang, David N. Ku, "A Nonlinear Axisymmetric Model with Fluid-Wall Interactions for Viscous Flows in Stenotic Elastic Tubes," *Journal of Biomechanical Engineering*, Vol. 121, pp. 494-501, 1999. (28 citations)

MAGAZINES AND LETTERS

- [18] Yan Luo, Jun Yang, Laxmi Bhuyan, Li Zhao, "NePSim: A Network Processor Simulator with Power Evaluation Framework," *IEEE MICRO, Special Issue on Network Processors for Future High-end Systems and Applications*, pp. 34-44, September, 2004. (32 citations)
- [19] Chuanjun Zhang, Frank Vahid, Jun Yang, Walid Najjar, "A Way-Halting Cache for Low-Energy High-Performance Systems," *IEEE Computer Architecture Letters*, Vol. 2, Iss. 1, 4 pages, September 2003.

CONFERENCE PUBLICATIONS

- [1] Lin Li, Youtao Zhang, Jun Yang, Jianhua Zhao, "Proactive NBTI Mitigation for Busy Functional Units in Out-of-Order Microprocessors," to appear, Design, Automation and Test in Europe, March, 2010.
- [2] Yi Xu, Bo Zhao, Youtao Zhang, Jun Yang, "Simple Virtual Channel Allocation for High throughput and High frequency On-chip Routers," to appear, The 16th International Symposium on High-Performance Computer Architecture (HPCA), January 2010. (acceptance rate: 18%)
- [3] Bo Zhao, Yu Du, Youtao Zhang, Jun Yang, "Variation-Tolerant Non-Uniform 3D Cache Management in Die Stacked Multicore Processor," to appear, The 42nd IEEE/ACM International Symposium on Microarchitecture, December 2009.
- [4] Ping Zhou, Bo Zhao, Jun Yang, Youtao Zhang, "Energy Reduction for STT-RAM Using Early Write Termination," to appear, *IEEE/ACM 2009 International Conference on Computer-Aided Design*, November, 2009. (acceptance rate: 115/438=26%)
- [5] Ping Zhou, Bo Zhao, Jun Yang, Youtao Zhang, "A Durable and Energy Efficient Main Memory Using Phase Change Memory Technology," *The 36th International Symposium on Computer Architecture (ISCA)*, pp. 14-23, June, 2009. (acceptance rate: 43/210=20%)
- [6] Yi Xu, Yu Du, Bo Zhao, Xiuyi Zhou, Youtao Zhang, Jun Yang, "A Low-Radix and Low-Diameter 3D Interconnection Network Design," *The 15th International Symposium on High-Performance Computer Architecture (HPCA)*, pp. 30-41, February 2009. (acceptance rate: 35/184=19%)
 - Best Paper Award Nominee
- [7] Ping Zhou, Bo Zhao, Yi Xu, Yu Du, Youtao Zhang, Jun Yang, Li Zhao, "Frequent Value Compression in Packet-based NoC Architectures," *The 14th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 13-18, January 2009. (acceptance rate: 116/355=33%)
- [8] Xiuyi Zhou, Yi Xu, Yu Du, Youtao Zhang, Jun Yang, "Thermal Management for 3D Processors via Task Scheduling," *The 37th International Conference on Parallel Processing (ICPP)*, pp. 115-122, September, 2008. (acceptance rate: 81/263=30%)

- [9] Jun Yang, Xiuyi Zhou, Marek Chrobak, Youtao Zhang, Lingling Jin, "Dynamic Thermal Management through Task Scheduling," *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, pp. 191-201, April, 2008. (acceptance rate: 22/63=35%)
- [10] Wei Wu, Jun Yang, Sheldon X.-D. Tan, Shih-Lien Lu, "Improving the Reliability of On-Chip Caches Under Process Variations," *IEEE International Conference on Computer Design (ICCD)*, pp. 325-332, October 2007. (acceptance rate: 88/259=33%)
- ▶ Best Paper Award (processor architecture track)
- [11] Jia Yu, Jinnan Yao, Laxmi Bhuyan, Jun Yang, "Program Mapping for Network Processors by Recursive Bipartitioning and Refining," *the 44th IEEE/ACM Design Automation Conference (DAC)*, pp. 805-810, June 2007. (acceptance rate: 161/713=23%)
- [12] Weijia Li, Youtao Zhang, Jun Yang, Jiang Zheng, "UCC: Update-conscious Compilation for Energy-efficiency in Wireless Sensor Networks," *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pp. 383-393, June 2007. (acceptance rate: 45/178 =25%)
- [13] Weijia Li, Youtao Zhang, Jun Yang, "Dynamic Authentication-key Reassignment for Reliable Report Delivery," *IEEE 3rd International Conference on Mobile Ad-hoc and Sensor Systems*, pp. 467-476, October 2006. (acceptance rate: 24%)
- [14] Lingling Jin, Wei Wu, Jun Yang, Chuanjun Zhang, Youtao Zhang, "Reduce Register File Leakage through Cell Discharging," *IEEE International Conference on Computer Design (ICCD)*, October 2006. (acceptance rate: 31%)
- [15] Lan Gao, Jun Yang, Marek Chrobak, Youtao Zhang, San Nguyen, Hsien-Hsin Lee, "A Low-cost Memory Remapping Scheme for Address Bus Protection," *the 15th IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pp. 74-83, 2006. (acceptance rate: 26%)
- [16] Wei Wu, Lingling Jin, Jun Yang, Pu Liu, Sheldon X.-D. Tan, "Efficient Method for Functional Unit Power Estimation in Modern Microprocessors," *the 43th IEEE/ACM Design Automation Conference (DAC)*, pp. 554-557, 2006. (acceptance rate: 209/865=24%)
- [17] Youtao Zhang, Jun Yang, Lingling Jin, Weijia Li, "Locating Compromised Sensor Nodes through Incremental Hashing Authentication," *IEEE International Conference on Distributed Computing in Sensor Systems (DCOSS)*, pp. 321-337, 2006. (acceptance rate: 30%)
- [18] Youtao Zhang, Jun Yang, Hai Vu, "Interleaved Authentication for Filtering False Reports in Multipath Routing Based Sensor Networks," *IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, April 2006. (acceptance rate: 23%)
- [19] Weidong Shi, Josh Fryman, Hsien-Hsin Lee, Youtao Zhang, Jun Yang, "InfoShield: A Security Architecture for Protecting Information Usage in Memory," *the 12th IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, pp. 225-234, February 2006. (acceptance rate: 14%)
- [20] Lingling Jin, Wei Wu, Jun Yang, Chuanjun Zhang, Youtao Zhang, "Dynamic Co-allocation of Resources for Level One Caches," *the 2nd International Conference on Embedded Software and Systems*, pp. 373-385, December 2005.
- [21] Jia Yu, Jun Yang, Shaojie Chen, Yan Luo, Laxmi Bhuyan, "Enhancing Network Processor Simulation Speed with Statistical Input Sampling," *2005 International Conference on High Performance Embedded Architectures & Compilers (HiPEAC)*, LNCS, Vol. 3793, pp. 68-83, 2005. (acceptance rate: 18%)
- [22] Pu Liu, Zhenyu Qi, Hang Li, Lingling Jin, Wei Wu, Sheldon X.-D. Tan, Jun Yang, "Fast Thermal Simulation for Architecture Level Dynamic Thermal Management," *IEEE International Conference on Computer-Aided Design (ICCAD)*, pp. 638-643, 2005. (acceptance rate: 25%)
- [23] Hang Li, Pu Liu, Zhenyu Qi, Lingling Jin, Wei Wu, Sheldon X.-D. Tan, Jun Yang, "Efficient Thermal Simulation for Run-Time Temperature Tracking and Management," *IEEE International Conference on Computer Design (ICCD)*, pp. 130-133, 2005. (acceptance rate: 101/313=32%)

- [24] Dinesh Suresh, Banit Agrawal, Walid Najjar, Jun Yang, "VALVE: Variable Length Value Encoding for Off-Chip Data Buses," *IEEE International Conference on Computer Design (ICCD)*, pp. 631-633, 2005. (acceptance rate: 101/313=32%)
- [25] Dinesh Suresh, Banit Agrawal, Walid Najjar, Jun Yang, "Tunable Bus Encoder for off-Chip Data Buses," *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 319-322, August 2005. (acceptance rate: 72/233=31%)
- [26] Yan Luo, Jia Yu, Jun Yang, Laxmi Bhuyan, "Low Power Network Processor Design Using Clock Gating," *the 42nd IEEE/ACM Design Automation Conference (DAC)*, pp. 712-715, June 2005. (acceptance rate: 154/735=20%)
- [27] Yongjing Lin, Youtao Zhang, Quanzhong Li, Jun Yang, "Supporting Efficient Query Processing on Compressed XML Files," *the 20th ACM Annual Symposium on Applied Computing (SAC)*, pp. 660-665, March 2005. (acceptance rate: 278/764=36%)
- [28] Jia Yu, Wei Wu, Xi Chen, Harry Hsieh, Jun Yang, F. Balarin, "Assertion-Based Automatic Design Exploration of DVS in Network Processor Architectures," *Design, Automation & Text in Europe (DATE)*, pp. 92-97, vol. 1, March 2005. (acceptance rate: 176/825=21%)
- [29] Youtao Zhang, Lan Gao, Jun Yang, Xiangyu Zhang, Rajiv Gupta, "SENS: Security Enhancement to Symmetric Shared Memory Multiprocessors," *the 11th IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, pp. 352-362, February 2005. (acceptance rate: 15%)
- [30] Chuanjun Zhang, Frank Vahid, Jun Yang, Walid Najjar, "A Way-Halting Cache for Low-Energy High Performance Systems," *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 126-131, August 2004. (acceptance rate: 70/204=34%)
- [31] Chuanjun Zhang, Jun Yang, Frank Vahid, "Low Static Power High Performance Frequent Value Data Caches," *Design, Automation & Text in Europe (DATE)*, pp. 214-219, February 2004. (acceptance rate: 23%)
- [32] Dinesh Suresh, Banit Agrawal, Jun Yang, Walid Najjar, Laxmi Bhuyan, "Power Efficient Encoding Techniques for Off-chip Data Buses," *ACM International Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES)*, pp. 267-275, October 2003. (acceptance rate: 31/162=19%)
- [33] Jun Yang, Youtao Zhang, Lan Gao, "Fast Secure Processors for Inhibiting Software Privacy and Tampering," *ACM/IEEE 36th International Symposium on Microarchitecture (MICRO)*, pp. 351-360, December 2003. (acceptance rate: 35/134=26%, 67 citations)
- [34] Dinesh Suresh, Jun Yang, Chuanjun Zhang, Banit Agrawal, Walid Najjar, "Reducing Transition Activity on Data Bas," *the 10th Annual International Conference on High Performance Computing (HiPC)*, pp. 44-54, December 2003. (acceptance rate: 48/164=29%)
- [35] Youtao Zhang, Jun Yang, "Procedural Level Address Offset Assignment of DSP Applications with Loops," *IEEE International Conference on Parallel Processing (ICPP)*, pp. 21-28, October 2003.
- [36] Jun Yang, Jia Yu, Youtao Zhang, "Lightweight Set Buffer: Low Power Data Cache for Multimedia Applications," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 270-273, August 2003. (acceptance rate: 90/221=41%)
- [37] Youtao Zhang, Jun Yang, "Low Cost Instruction Cache Design for Tag Comparison Elimination," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 266-269, August 2003. (acceptance rate: 90/221=41%)
- [38] Jun Yang, Rajiv Gupta, "Energy Efficient Frequent Value Data Cache Design," *ACM/IEEE the 35th International Symposium on Microarchitecture (MICRO)*, pp. 197-207, November 2002. (acceptance rate: 36/150=24%, 45 citations)

- [39] Jun Yang, Rajiv Gupta, "FV Encoding for Low-Power Data I/O," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 84-87, August 2001. (acceptance rate: 73/194=38%, 22 citations)
- [40] Jun Yang, Rajiv Gupta, "Energy-Efficient Load and Store Reuse," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 72-75, August 2001. (acceptance rate: 73/194=38%)
- [41] Jun Yang, Youtao Zhang, Rajiv Gupta, "Frequent Value Compression in Data Caches," *ACM/IEEE the 33rd International Symposium on Microarchitecture (MICRO)*, pp. 258-265, December 2000. (acceptance rate: 31/110=28%, 70 citations)
- [42] Youtao Zhang, Jun Yang, Rajiv Gupta, "Frequent Value Locality and Value-Centric Data Cache Design," *ACM 9th International Conference on Architecture Support for Programming Languages and Operating Systems (ASPLOS)*, pp. 150-159, November 2000. (acceptance rate: 24/114=21%, 76 citations)
- [43] Jun Yang, Rajiv Gupta, "Load Redundancy Removal through Instruction Reuse," *IEEE International Conference on Parallel Processing (ICPP)*, pp. 61-68, August 2000.

REFEREED WORKSHOP PUBLICATIONS

- [1] Lin Li, Xiuyi Zhou, Jun Yang, Victor Puchkarev, "ThresHot: An Aggressive Task Scheduling Approach in CMP Thermal Design", *Workshop on Unique Chips and Systems, in conjunction with ISPASS2009*, April, 2009.
- [2] Jia Yu, Wei Wu, Xi Chen, Harry Hsieh, Jun Yang, F. Balarin, "Assertion-Based Power/ Performance Analysis of Network Processor Architectures," *IEEE International High Level Design Validation and Test Workshop*, November 2004.
- [3] Youtao Zhang, Jun Yang, Yongjing Lin, Lan Gao, "Architectural Support for Protecting User Privacy on Trusted Processors," *The Workshop on Architectural Support for Security and Anti-Virus, in conjunction with the 11th ASPLOS*, pp. 114-119, October 2004.

TEACHING EXPERIENCE

New Course Developed

ECE 2162 Computer Architecture (Spring 2007, University of Pittsburgh)

This course was fully upgraded to focus on the latest developments in microarchitecture. Apart from techniques in the textbook, students were exposed to design details of commercial high-end microprocessors such as Pentium 4 from Intel. In addition, major research infrastructures such as SimpleScalar and Simics were introduced in classroom and students were requested to use them in exercises. Extensive programming projects on instruction scheduling, out-of-order execution, and superscalar pipeline were developed for students to learn the in-depth designs of real processors. Research articles were also incorporated as course material and extra readings for students.

ECE 2195 Modern Computer Processor and System Architecture (Fall 2007, University of Pittsburgh)

Dr. Yang developed this new course for senior level graduate students to broaden their view in computer architecture. This course covers the most up-to-date technologies in planar multi-core and 3D chip architecture. The latest research articles were extensively discussed as the main course material. Dr. Yang designed new projects that cover the important aspects such as power and thermal management, interconnection network and cache management in CMP and 3D chips. Students were trained with the widely used research tools such as Simics, SimpleScalar, HotSpot, Orion, Cacti. Circuit level designs were also heavily incorporated in the projects.

CSE 260 Computer Architecture Seminar (Winter 2003, Spring 2005, University of California Riverside)

This course was offered once every two years, with a goal to cover the latest technologies developed in the last two years. In the first offer in 2003, Dr. Yang developed a syllabus that incorporated low power techniques in cache memories, buses; frequent value compression and encoding (Dr. Yang's thesis research); simultaneous multithreading technique; and network processor architectures. Dr. Yang designed a set of projects related to the above lectured topics. Most of the projects resulted in conference and journal publications. The network processor project later developed into a Ph.D. thesis topic for Dr. Yan Luo. In the 2005 offering, Dr. Yang developed material that covers in-depth design details of secure processors, memory protection and information flow tracking. The students were asked to simulate and evaluate the impact of various memory encryption/decryption and authentications schemes on the performance of a program.

CSE162 Computer Architecture (Spring 2006, University of California Riverside)

This course was developed to bridge the gap between its prerequisite CSE161 which covers the fundamentals in computer organization, and the entry level graduate computer architecture course CSE203A which covers more advanced material in computer architecture. This course was designed to include the data path and control path of pipelined architecture, including pipeline stall, forwarding, and flush; memory management including paging and virtual memory; multiprocessors and interconnection topologies; I/O systems; and network designs.

University of Pittsburgh

ECE 2195	Modern Computer Processor and System Architecture (advanced graduate level)	Spring 2009	Enrollment: 9
ECE 2162	Computer Architecture	Fall 2008	Enrollment: 10
CoE/ECE 0142	Computer Organization (undergraduate level)	Spring 2008	Enrollment: 35
ECE 2195	Modern Computer Processor and System Architecture (advanced graduate level)	Fall 2007	Enrollment: 11
ECE 2162	Computer Architecture (introductory graduate level)	Spring 2007	Enrollment: 19
CoE/ECE 0142	Computer Organization (undergraduate level)	Fall 2006	Enrollment: 20

University of California Riverside

CSE162	Computer Architecture (undergraduate level)	Spring 2006	Enrollment: 10
CSE161	Design and Architecture of Computer Systems (undergraduate level)	Winter 2006	Enrollment: 21
CSE161	Design and Architecture of Computer Systems (undergraduate level)	Fall 2005	Enrollment: 34
CSE260	Computer Architecture Seminar	Spring 2005	Enrollment: 4

	(advanced graduate level)			
CSE161	Design and Architecture of Computer Systems (undergraduate level)	Winter 2005	Enrollment: 16	
CSE203A	Computer Architecture (introductory graduate level)	Fall 2004	Enrollment: 33	
CSE161	Design and Architecture of Computer Systems (undergraduate level)	Spring 2004	Enrollment: 63	
CSE161	Design and Architecture of Computer Systems (undergraduate level)	Winter 2004	Enrollment: 60	
CSE203A	Computer Architecture (introductory graduate level)	Fall 2003	Enrollment: 42	
CSE260	Computer Architecture Seminar (advanced graduate level)	Winter 2003	Enrollment: 12	
CSE203A	Computer Architecture (introductory graduate level)	Fall 2002	Enrollment: 28	

PROFESSIONAL SERVICE ACTIVITIES

Conference/Workshop Organization Committee

1. Finance and Registration Chair – Fifteenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'10), Pittsburgh, PA, Mar. 2010.
2. Finance and Registration Chair – IEEE Computer Society Annual Symposium on VLSI, 2009, Tampa, FL, May 2009.
3. Workshop/Tutorials Chair – 2009 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), Boston, MA, Apr. 2009.
4. Program Chair – The 12th Workshop on Interaction between Compilers and Computer Architecture (Interact-12), in conjunction with the 14th International Symposium on High-Performance Computer Architecture (HPCA14), Salt Lake City, Utah, Feb. 2008.
5. Program Chair – The 16th International Conference on Computer Communications and Networks, Computer Architecture for Networking and Communications Track, Honolulu, Hawaii, Aug. 2007.
6. Program Chair – The International Conference on Embedded and Ubiquitous Computing (EUC), Embedded System Architecture Track, Seoul, Korea, Aug. 2006.

Technical Program Committee Member

1. 21st International Symposium on Computer Architecture and High Performance Computing, computer architecture track, Sao Paulo, Brazil, Oct. 2009.
2. The 3rd Workshop on Chip Multiprocessor Memory Systems and Interconnects, in conjunction with 36th International Symposium on Computer Architecture (ISCA), Austin, TX, Jun. 2009.
3. Workshop on Unique Chips and Systems (UCAS-5), in conjunction with IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) 2009, Boston, MA, Apr. 2009.
4. International Symposium on Low Power Electronics and Design (ISLPED), Bangalore, India, Aug. 2008.
5. The 13th Asia and South Pacific Design Automation Conference (ASP-DAC), Student Forum, Jan. 2008.

6. Workshop on the Interaction between Operating Systems and Computer Architecture, in conjunction with the 35th International Symposium on Computer Architecture (ISCA), Beijing, China, Jun. 2008.
7. The 14th IEEE International Conference on High Performance Computing (HiPC), Goa, India, Dec. 2007.
8. International Symposium on Low Power Electronics and Design (ISLPED), Portland, Oregon, Aug. 2007.
9. Workshop on the Interaction between Operating Systems and Computer Architecture, in conjunction with the 34th International Symposium on Computer Architecture (ISCA), San Diego, California, Jun. 2007.
10. The 2nd International Conference on Embedded Software and Systems, Xian, China, Dec. 2005.
11. ACM SIGPLAN/SIGBED 2005 Conference on Language, Compilers, and Tools for Embedded Systems (LCTES), Jun. 2005.
12. The 10th IEEE International Conference on High Performance Computing (HiPC), Hyderabad, India, Dec. 2003.

NSF Panelist

1. NSF Cyber Trust, April 2005
2. NSF Foundations of Computing Processes and Artifacts Cluster, March 2008
3. NSF CAREER, October 2008
4. NSF CAREER, October 2009

Conference/Workshop Session Chair

1. International Symposium on Performance Analysis of Systems and Software, April 2008
2. Workshop on the Interaction between Operating Systems and Computer Architecture, in conjunction with the 35th International Symposium on Computer Architecture (ISCA), Beijing, China, Jun. 2008
3. ACM/IEEE International Symposium on Low Power Electronics and Design, August 2007

Reviewer for

IEEE Transactions on Computers, 2000 – 2009

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 2005 – 2008

IEEE Transactions on Very Large Scale Integrated Systems 2005 – 2008

IEEE Transactions on Parallel and Distributed Systems 2007

IEEE MICRO 2002 – 2009

IEEE Computer Architecture Letters 2005 – 2008

ACM (Association of Computing Machinery) Transactions on Design Automation of Electronic Systems 2002 – 2008

ACM Transactions on Architecture and Code Optimization 2002 – 2009

ACM Transactions on Embedded Computing Systems 2002 – 2008

Elsevier Journal of Computer Languages, Systems & Structures 2007

Journal of VLSI Signal Processing Systems 2006

International Symposium on Computer Architecture (ISCA) 2006 – 2008

International Symposium on Microarchitecture (MICRO) 2001 – 2008

International Symposium on High Performance Computer Architecture (HPCA) 2008

ACM SIGPLAN Conference on Program Language Design and Implementation (PLDI) 2004

International Conference on Compilers, Architecture, Synthesis for Embedded Systems (CASES) 2004 – 2006

Design, Automation & Test in Europe (DATE) 2004 – 2006

International Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS) 2003 – 2004

INVITED PRESENTATIONS

1. "Frequent Value Compression in Packet-based NoC Architectures," given at the 14th Asia and South Pacific Design Automation Conference, Yokohama, Japan, January 2009.
2. "A Low-Radix and Low-Diameter 3D Interconnection Network Design," given at the Computer Science and Technology Department, Nanjing University, Nanjing, China, December, 2008.
3. "A Low-Radix and Low-Diameter 3D Interconnection Network Design," given at the Computer Architecture Lab at Carnegie Mellon (CALCM), ECE Department, Carnegie Mellon University, November, 2008.
4. "Dynamic Thermal Management through Task Scheduling," given at the 2008 IEEE International Symposium on Performance Analysis of Systems and Software, Austin, TX, Apr. 2008.
5. "Dynamic Thermal Monitoring and Management for High-Performance Microprocessor," given at the Intel Research Lab, Pittsburgh, Feb. 2007.
6. "Dynamic Power and Thermal Monitoring and Managements for High-Performance Microprocessors," given at the Intel Asia-Pacific Research Development, Ltd. Shanghai, China, Dec. 2006.
7. "Dynamic Power and Thermal Monitoring and Managements for High-Performance Microprocessors," given at the School of Microelectronics, Shanghai Jiaotong University, Shanghai, China, Dec. 2006.
8. "Dynamic Power and Thermal Monitoring for High-Performance Microprocessors," given at the Computer Science Department, University of Pittsburgh, Dec. 2006.
9. "Dynamic Power and Thermal Monitoring for High-Performance Microprocessors," given at the Department of Computer Science and Engineering, Pennsylvania State University, Oct. 2006.
10. "Frequent Value Phenomenon and its Applications," given at the Department of Computer Science and Engineering, University of California Riverside, May, 2002.
11. "Frequent Value Phenomenon and its Applications," given at the Department of Computer Science and Engineering, University of Texas Arlington, Apr. 2002..
12. "Frequent Value Phenomenon and its Applications," given at the Department of Computer Science and Engineering, University of North Texas, Apr. 2002.
13. "Frequent Value Phenomenon and its Applications," given at the Computer Science Department, Rutgers, the State University of New Jersey, Apr. 2002.
14. "Frequent Value Phenomenon and its Applications," given at the Department of Computer Science, State University of New York Binghamton, Apr. 2002.
15. "Frequent Value Phenomenon and its Applications," given at the Department of Computer Science and Engineering, University of Connecticut, Mar. 2002.
16. "Frequent Value Phenomenon and its Applications," given at the Department of Computer and Information Sciences, University of Delaware, Mar. 2002.
17. "FV Encoding for Low-Power Data I/O," given at the ACM/IEEE International Symposium on Low Power Electronics and Design, Huntington Beach, CA, Aug. 2001.
18. "Energy-Efficient Load and Store Reuse," given at the ACM/IEEE International Symposium on Low Power Electronics and Design, Huntington Beach, CA, Aug. 2001.
19. "Frequent Value Compression in Data Caches," given at the ACM/IEEE 33rd International Symposium on Microarchitecture, Monterey, CA, Dec. 2000.
20. "Load Redundancy Removal through Instruction Reuse," given at the International Conference on parallel Processing, Toronto, Canada, Aug. 2000.

Internal Presentations

1. "Architectural Design and Consideration for 3D Chip Multiprocessors," given at the ECE Department Undergraduate Seminar, Sept. 2006.

2. "Dynamic Power and Thermal Monitoring and Managements for High-Performance Microprocessors," given at the ECE Department Graduate Seminar, Oct. 2006.
3. "Towards an Energy and Thermally Efficient High-Performance Microprocessor Design," given at the ECE Department Undergraduate Seminar, Nov. 2006.
4. "Low Power and Thermal Management for High-Performance Microprocessor Designs," given at the IEEE Chapter, Undergraduate Seminar ECE Department, Nov. 2006.

DEPARTMENTAL ADMINISTRATIVE ACTIVITIES

COMMITTEES

1. Graduate committee, ECE Dept. of Pittsburgh, 2009-2010.
2. Faculty recruiting committee, ECE Dept. University of Pittsburgh, 2008-2009.
3. Graduate admission, computer engineering area, ECE Dept., University of Pittsburgh, 2006-2007.
4. Graduate admission committee, Dept. of Computer Science and Engineering, University of California Riverside, 2005 – 2006.
5. Faculty recruiting committee, Dept. of Computer Science and Engineering, University of California Riverside, 2003 – 2005.

DISSERTATION/THESIS COMMITTEE

University of Pittsburgh: Gerold Joseph (MS), Colin Ihrig (MS and PhD), Gayatri Mehta (PhD), Justin Stander (MS), Ruibin Xu (PhD), Mohammad Hammoud (PhD), Taecheol Oh (PhD), Hunjin Lee (PhD)

University of California Riverside: Jinnan Yao (PhD), Jiani Guo (PhD), Dinesh Suresh (PhD), Li Zhao (PhD), Susan Lysecky (PhD), Roman Lysecky (PhD), Ann Gordon-Ross (PhD), Greg Stitt (PhD), Chuanjun Zhang (PhD), Xi Chen (PhD), Jessica Lin (PhD), Chotirat (Ann) Ratanamahatana (PhD), Xiaopeng Xi (PhD), Junjie Yang (PhD)

Georgia Institute of Technology: Tao Zhang (PhD) – external member

College of William and Mary: Zhichun Zhu (PhD) – external member